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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/040,055	12/31/2001	James K. Falbo	NTI-030	1929

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EXAMINER	
ROSSOSHEK, YELENA	
ART UNIT	**PAPER NUMBER**
2825	

DATE MAILED: 04/02/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/040,055	FALBO ET AL.	
	Examiner	Art Unit	
	Helen B Rossoshek	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 January 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-54* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10,12-32,34-36 and 44-54* is/are rejected.

7)☒ Claim(s) *11,33 and 37-43* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *31 December 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to the application 10/040,055 filed 12/11/2001 and amendment filed 01/05/2004.

2. Claims 1-54 remain pending in the application.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1-10, 12-32, 34-36 and 44-54 are rejected under 35 U.S.C. 102(e) as being anticipated by Agrawal et al. (US Patent 6,523,162).

The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

As to claims 1, 12 and 32 Agrawal et al. teaches performing a layout beautification operation on an integrated circuit (IC) layout comprising a plurality of polygons, comprising applying a first action to a first portion of the IC layout responsive

to determining that a first shape associated with the first action matches the first portion of the IC layout, the first shape comprising at least a first edge and a second edge related according to a defined property, the first shape being configured to match a first type of layout imperfection wherein the layout features comprises the polygon or groupings of polygons representing the layout imperfection (col. 14, ll.20-31); defining a plurality of shapes, each of the plurality of shapes comprising at least first edge and a second edge related according to at least one of a plurality of defined properties, each of the plurality of shapes matching at least one of the plurality layout imperfections as shown on the Fig.4a-Fig.4c; defining a plurality of actions to correct the plurality of layout imperfections, each of the plurality of actions being associated with at least one of the plurality of shapes (col. 8, ll.49-59); and applying the plurality of actions to the IC layout responsive to the at least one of the plurality of shapes associated with each of the plurality of actions matching elements within the IC layout (col. 8, ll.59-61); a software program comprising: a first set of instructions for comparing a first shape to the plurality of features in each of the plurality of polygons to identify a first set of matching layout features, the first shape comprising at least a first edge and second edge related according to a first property; and a second set of instructions for performing a first layout beautification action on each of the first set of matching layout features (col. 14, ll.20-31; col. 8, ll.39-42).

As to claims 2-10 and 34-36 Agrawal et al. teaches the first action comprising adjusting the first type of layout imperfection by a fixed amount as shown on the Fig. 9c (col. 10, ll.65-67); the first type of layout imperfection covers a plurality of actual layout

imperfections, each of the plurality of actual layout imperfections having a different set of actual properties, wherein the first action comprises making an adjustment according to the set of actual properties for each of the plurality of actual layout imperfections according the catalog of shapes and specified actions (as functions of the properties of the shapes) listed in the Table 2 (col. 14, ll.24-27); the first action comprises replacing the first type of layout imperfection with a second shape within the bias table containing a set of actions based on a catalog of shapes (col. 10, ll.37-47); the first edge and the second edge are not contiguous (col. 14, ll.43-45; col. 18, ll.33-34); the IC layout comprises a first layer and a second layer, the first edge being associated with the first layer, and the second edge being associated with the second layer (col. 3, ll.30-32); first layer comprises a gate layer, and wherein the second layer comprises a wire layer (col. 7, ll.27-28; 35-37; 39-40); defined property specifies a plurality of alternative relationships between the first edge and the second edge by using wildcard as shown on the Fig. 7d (col. 8, ll.18-21; ll.25-26; col. 14, ll.21-23); the second edge being contiguous with and substantially perpendicular to the first edge, and wherein the first shape further comprises a third edge, the third edge being contiguous with and substantially perpendicular to the second edge, the third edge being substantially parallel to and side-by-side with the first edge (col. 16, ll.64-67; col. 17, ll.1-4); the second edge being contiguous with and substantially perpendicular to the first edge, and wherein the first shape further comprises: first edge, the third edge being contiguous with and substantially perpendicular to the second edge, wherein the third edge is not substantially side-by-side with the first edge as shown on the Fig. 6e and

Fig. 7d; a fourth edge, the fourth edge being contiguous with and substantially perpendicular to the third edge, wherein the fourth edge is not substantially side-by-side with the second edge as shown on the Fig. 6e; a fifth edge, the fifth edge being contiguous with and substantially perpendicular to the fourth edge, wherein the fifth edge is substantially parallel to and side-by-side with the third edge as shown on the Fig. 6e; a sixth edge, the sixth edge being contiguous with and substantially perpendicular to the fifth edge, wherein the sixth edge is not substantially side-by-side with the fourth edge as shown on the Fig. 6e; and a seventh edge, the seventh edge being contiguous with and substantially perpendicular to the sixth edge, the seventh edge being substantially parallel to and side-by-side with the first edge as shown on the Fig. 6e.

As to claims 13-18 Agrawal et al. teaches the plurality of actions having a specified sequence, wherein any element within the IC layout to which one of the plurality of actions is applied is excluded from further applications of the plurality of actions within the process being sequential or batch mode (abstract); the specified sequence being determined according to a predefined ranking of layout imperfection criticality wherein the order of the shape matching operation is set by user (col. 4, ll.18-27); applying the plurality of actions to the plurality of elements included in a first polygon in the plurality of polygons in a specified sequence within identifying the layout features if interest (polygon or groupings of polygons) (col. 3, ll.23-26; col. 4, ll.18-21); restarting the specified sequence when one of the plurality of actions is applied to one of the elements of the IC layout included in the first polygon as shown on the Fig. 8

within the loop A according the sequential actions operation (col. 10, ll.37-47); applying the first action to the IC layout responsive to the at least one of the plurality of shapes associated with the first action matching elements in the IC layout; and applying a second action to the IC layout responsive to the at least one of the plurality of shapes associated with the second action matching elements in the IC layout (col. 9, ll.46-56); applying each of the plurality of actions to a first polygon in the plurality of polygons (Fig. 5a-5d; Fig. 6e) responsive to the at least one of the plurality of shapes associated with each of the plurality of actions matching elements in the first polygon (col. 10, ll.37-47); applying each of the plurality of actions to a second polygon in the plurality of polygons responsive to the at least one of the plurality of shapes associated with the plurality of actions matching elements in the second polygon (layout feature) (col. 11, ll.26-33); initialization a lookup table, the lookup table incorporating the plurality of actions (abstract; col. 2, ll.33-34).

As to claims 19-31 Agrawal et al. teaches an input data manager for loading the IC layout data file into the system as shown on the Fig. 10a (col. 12, ll.17-22); a layout beatification engine for applying a plurality of corrective actions to the IC layout data file responsive to at least one of a plurality of shapes associated with each of the plurality of corrective actions matching elements in the IC layout data file, wherein each of the plurality of shapes comprises at least a first edge and a second edge related according to at least one of a plurality of defined properties within OPC engine (1030) shown on the Fig. 10a (col. 12, ll.49-60); an output data manager for generating an output data file within (1040) shown on the Fig. 10a (col. 13, ll.30-32); within the data manager which

might divide the data file (col. 12, ll.28-33; Fig. 10a); a first data file format, wherein loading the IC layout data file into the system comprises converting the first data file format into a second data file format, the layout beautification engine being configured to operate on the second data file format (col. 12, 23-27; ll.28-33; ll. 36-38; Fig. 10a); generating the output data file comprises converting the second data file format into a third data file format within the hierarchy manager (1020) shown on the Fig. 10a which might decrease the size of the file (col. 12, ll.41-48); the layout beautification engine comprises a lookup table incorporating the plurality of corrective actions within the bias table (abstract; col. 2, ll.33-34); a network connection to a remote storage location, wherein the remote storage location stores at least one of the IC layout data file and the plurality of corrective actions within the storage (1190) shown on the Fig. 11 (col. 13, ll.51-56); the plurality of corrective actions are incorporated in a lookup table (abstract; col. 2, ll.33-34).

As to claims 44 and 45 Agrawal et al. teaches identifying a shape pattern in the input layout by identifying layout features of interest (col. 12, ll.21); replacing the identified shape pattern with an alternative configuration, the alternative configuration reducing data volume within hierarchy manager (1020) shown on the Fig. 10a (col. 12, ll.41-48); the alternative configuration provides one of an absolute correction, an adaptive correction and a replacement correction within model-based actions (when fixed value adjustment is made), rule-based actions (when adjustment depends on actual characteristics) and shape-based actions (when action with replacement shapes) respectively (abstract).

As to claims 46-54 Agrawal et al. teaches identifying shape patterns on the layout (abstract); modifying the layout according to corrective actions associated with the identified shape patterns, wherein the corrective actions include at least one of: performing a first operation using a fixed value associated with an existing layout parameter of an identified shape pattern; performing a second operation that is a function of an existing layout parameter of an identified shape pattern; performing a third operation that replaces an identified shape pattern (col. 4, ll.45-50); the first operation includes matching a dimensional specification of a design rule and the existing layout parameter (abstract); performing the first operation includes fixed biasing (abstract; col. 1, ll.65-67; col. 2, ll.1-3); performing the second operation includes providing a corrective action proportional to the existing layout parameter (col. 8, ll.37-48); performing the second operation includes at least one of proportional biasing and negative biasing (col. 1, ll.53-57; col. 2, ll.7-12; col. 16, ll.1-3); the replacement correction replaces the identified shape pattern with a simplified shape pattern within the hierarchy manager (1020) shown on the Fig. 10a (col. 41, ll.41-48).

Remarks

5. Applicant's definition of the layout imperfection is broad, that gives a space for other definitions of the layout imperfection. The fact that Applicant placed this information in the background of the specification is evidence that layout imperfection is widely known by one of ordinary skill in the art to exist in layout imperfection where OPC actions are equivalent. The prior art reference (Agrawal et al.) discloses the use of OPC to compensate for layout distortions introduced by the exposure process (col. 1, ll.33-

39). This distortions are layout imperfections; and Agrawal et al. teaches OPC actions, by definition could not be performed, unless layout imperfections exist a prior (col. 2, ll.13-20; col. 3, ll.23-30). Additionally, Applicants assert that Agrawal et al. does not teach a layout beautification engine. Applicant's specification fails to teach a specific definition of a layout beautification engine. However Applicant's specification discloses the functionality of the layout beautification engine. Agrawal et al. teaches OPC engine depicted on the Fig. 10b in details, which is a part of the OPC system (1000) shown on the Fig. 10a, wherein the OPC engine directly corresponds to the functions of Applicant's beautification engine in respect of the name. Applicants are entitled to use their own terms, so OPC engine might be called by different name. The fact is that OPC engine and layout beautification engine have equivalent functions. Moreover with respect to claim 32 Agrawal et al. discloses a second set of instructions for performing a first layout beautification action on each of the first set of matching layout features as a code (program) which is a part of the modification system wherein the shapes/actions might be provided by system automatically or executed manually by the user (col. 8, ll.51-54; col. 20, ll.23-24). With respect to claim 44 Agrawal et al. teaches the apparatus comprising: means for identifying a shape pattern in the input layout, wherein the shape pattern comprises at least a first edge and a second edge related according to at least one of a plurality of defined properties using a data controller (1032), which is a part of the OPC engine, shown on the Fig. 10b for accepting a set of geometries (wherein a set of geometries might only include a single polygon having at least a first edge and a second edge demonstrated on the Figs. 4a-4c (col. 6, ll.35-43)) and separating the data

into primitives, which reduces the size of the data for inputting into shape scanner (1034) (col. 12, ll.54-57; col. col. 15, ll.44-46). Agrawal et al. further teaches identifying a shape pattern on a layout (abstract) and applying an adaptive correction to the identified shape pattern (col. 8, ll.37-48).

Allowable Subject Matter

6. Claims 11, 33 and 37-43 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. The prior art of record does not teach a third set of instructions: the second edge being contiguous with and substantially perpendicular to the first edge, and wherein the first shape further comprises: a third edge, third edge being contiguous with and substantially perpendicular to the second edge; a fourth edge being contiguous with and substantially perpendicular to the third edge; and a fifth edge being contiguous with and substantially perpendicular to the fourth edge, wherein none of the first edge, the second edge, the third edge, the fourth edge, and the fifth edge are substantially side-by-side with each other; for defining the first shape according to a set of user inputs; for loading the first shape from across a network, for defining the first layout beatification action according to a set of user inputs; for loading the first action from across a network; for comparing a second shape to the plurality of features in each of the plurality of polygons to identify a second set of matching layout features, the second shape comprising at least a third edge and fourth edge related according to a second property; and fourth set of instructions for performing a second layout beatification action on the second set of

matching layout features; the first set of instructions and the second set of instructions are completely executed before the third set of instructions and the fourth set of instructions; the first set of instructions and the second set of instructions are executed concurrently, and wherein comparing the first shape to a selected one of the plurality of features in each of the plurality of polygons is performed before comparing the second shape to the selected one of the plurality of features in each of the plurality of polygons.

7. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Helen B Rossoshek whose telephone number is 571-272-1905. The examiner can normally be reached on 7:00-4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew S Smith can be reached on 571-272-1907. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

HR